

100G Pluggable Optics Drive Testing in New Directions

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Introduction

With 100G products now becoming a reality, client interfaces based on CFP optics are appearing on routers, switches, and transport equipment. Although the technology is maturing, the complexity and performance of pluggable optics remains challenging and is compounded by the relative short supply and high cost of the CFPs.

Traditionally, Ethernet optics have been reliable components, but the increased technical complexity of 100G optics requires testing and screening them both during the vendor selection and production.

This white paper introduces CFP optics and highlights the tests and measurements required to validate them.

The equipment described in this white paper is currently available from JDSU. For further details, please visit our website (www.jdsu.com), or contact any of our local sales team.

Transponder Overview

The main transponders used for 40 and 100 Gigabit Ethernet (GE) are listed in the table, other vendors also may offer transponders in CFP form-factor. JDSU does not endorse or provide support for any particular vendor.

The IEEE 802.3ba defines a system based on four wavelengths for long reach (LR4) at 40G and 100G, while Santur offers a 10-lambda-based optic that is not photonically compatible with the LR4 standard but does comply with the CFP Multisource Agreement (MSA).

Type	Notes	Reach	Wavelength	Nominal Cost <i>(prices for magnitude comparison)</i>
100G				
10 x 10 Gbps (SR10)	Uses parallel optics (both CFP and CXP form-factor)	~100 m	850 nm x 10	N/10
10 x 10 Gbps	Non-standard Santur	10 km+	1550 nm – 10λ	N
4x25 Gbps (LR4)	IEEE standard, requires a gearbox	10 km	1310 nm – 4λ	3N
4x25 Gbps (ER4)	IEEE standard, requires a gearbox	40 km	1310 nm – 4λ	3N
40G				
4 x 10 Gbps (LR4)	No gearbox required	10 km	1310 nm – 4λ	N/8
40G Serial (FR)	Requires a SERDES, must be compatible with 40G 300-pin MSA-based optics	10 km	1550 nm – 1λ	N/2
40G (SR4)	CFP and QSFP+ form-factor	~100 m	850 nm x 4	N/20

Note that the nominal cost is only a rough indication of the relative magnitude of costs for the optics and can be subject to change when optics meet maturity and enter mass deployment.

The short reach optics (SR) use multimode fibers and virtual cavity surface-emitting laser (VCSEL) arrays to transmit the 40G/100G signal over parallel fibers. Although the cost of the SR optics is much lower (typically <1/10) than the cost of the LR optics, concerns exist about the parallel optical ribbon cables, such as cost, new infrastructure, inspection, and cleaning of connectors.

The 40G serial (FR) case is focused on compatibility with legacy 40G serial 300-pin MSAs (typically used in SONET/SDH deployments). Many large operators like the concept of a universal 40G port that can support multiple technologies (legacy SONET/SDH/OTN and 40GE). They have already deployed 40G based on the 300-pin (fixed optics based on an electrical 17 x 2.5G interface = 16 + 1 deskew lane). The 40G serial is still not considered a mainstream, cost-effective technology (despite its introduction in 2000). The upper limit for practical serial transmission (based on integrated circuit [IC] technology and laser physics) is around 28G. The 40G serial optics will likely be deployed only in cases where operators have already deployed 40G serial, as the price of the serial optics will likely remain approximately three times higher than the 40G parallel.

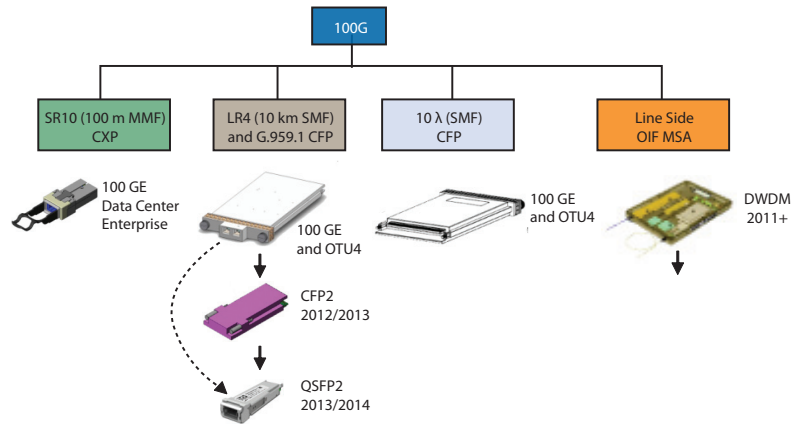


Figure 1. 100G Optics Family Tree

As you can see, the plan is to migrate away from the CFP form-factor over the next few years, which is expected to begin in early 2011 for 40 GE to Quad Small Form-Factor Pluggable Plus (QSFP+). The 100G technology will take longer as challenges remain over the 25G/28G electrical interface and photonic integration required to support a smaller form-factor at that rate. The CXP form-factor is already establishing itself as a strong contender in the Enterprise space because of its low cost and compact form-factor.

Figure 2 shows the internal functions of a 100G LR4 transponder.

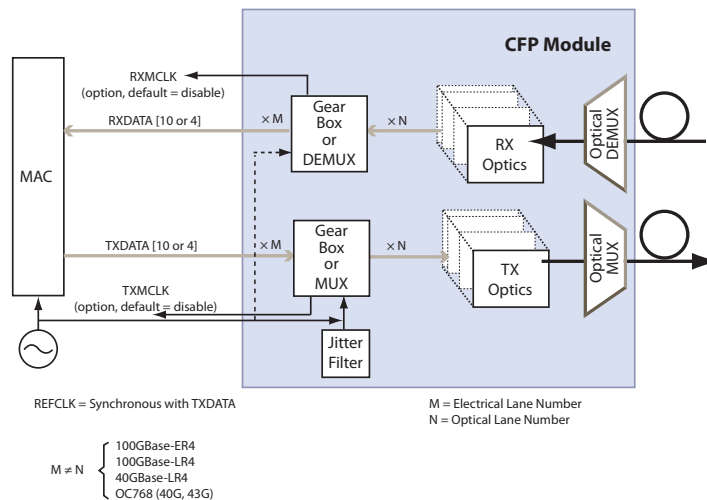


Figure 2. Internal function of a 100G LR4 transponder

The gearbox IC is a chipset that converts the 10 x 10G electrical lanes into 4 x 25G lanes and vice-versa for the receiver side. The laser (Tx) optics requires four lasers, each with 5-nm spacing with the corresponding modulating and thermal management circuitry.

An optical mux brings together the four separate transmit lambdas onto one single-mode fiber. On the receive side an optical demux splits the incoming signal into four separate lambdas, which in turn are received by a photodiode and amplifier assembly. A clock data recovery (CDR) will be used on one of the receive channels to provide a recovered clock for the demux gearbox.

Of course, a 40 GE parallel CFP does not need a gearbox, because they provide a 1:1 correspondence between electrical and optical lanes.

The host (electrical) interface is based on either 10 (100G) or 4 (40G) electrical lanes running at ~10.3125G for Ethernet applications (slightly higher for OTU3/4 rates) and a clock (reference clock, or refclk). Unlike legacy interfaces such as SFI 5.1 that rely on a separate deskew lane, the 40 GE and 100 GE encoding uses embedded deskew information, which has been (re)used for OTU3/4 with the concept of OTL virtual lane rotation, and 40G SONET can use STL256.4 for backwards compatibility with STM256 serial 40G.

Module command and control uses a high-speed serial management data input/output (MDIO) bus, which allows monitoring and control of many internal functions such as optical power, temperature, and vendor identification (ID).

The integration of so many complex, high-speed photonics and electronics inside a CFP module remains challenging as do thermal management, stability, performance, and manufacturability.

The gearbox IC requires special attenuation due to the electrical performance of the high-speed interfaces which are extremely demanding, especially the parallel host interface. Managing 10 parallel 10G electrical signals for individual and relative timing presents significant issues, such as crosstalk, relative dynamic skew, jitter, and eye closure, in module integration.

Note that the top surface is designed to provide good thermal contact with the riding heatsink.

Figure 4 illustrates a comprehensive CFP test system based on the Optical Network Transport (ONT) and Multiple Application Platform (MAP) product lines. A Hydra 100G stressor is also in use but is not shown.

The top center of the figure shows an ONT 100G system running full rate 100G Ethernet traffic while simultaneously adding physical layer stresses, such as dynamic skew. The second shelf shows a MAP platform performing the lambda demux/mux function to enable monitoring or attenuating of individual wavelengths (scope on right shows individual 25G eye). A T-BERD®/MTS-8000 shows the complete optical spectrum. Figure 5 shows the electrical interface side.

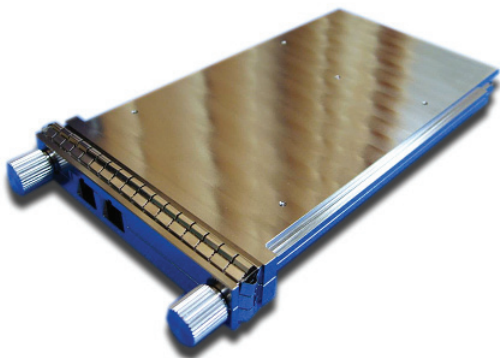


Figure 3. A 100G CFP module



Figure 4. Comprehensive CFP Test System

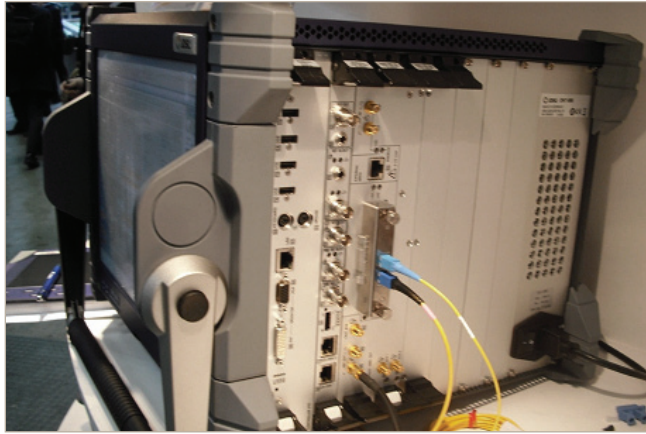


Figure 5. Electrical interface for testing

The high-speed electrical interface uses parallel 10G lanes (either 4 or 10), each running as a differential signal (receive [Rx] and transmit [Tx]). Various clock signals are also running at subrates of the data lines (typically 1/16 lane speed or approximately 644 MHz) as well as control pins (dedicated and MDIO) and power.

Clearly the bulk of the test validation should focus on the functionality and signal integrity of the high-speed parallel data bus, but it is also important to validate the control pin functionality, especially the MDIO bus.

Unframed PRBS and Digital Word

An unframed pseudorandom bit sequence (PRBS) and digital word provides the basis of first-pass testing for hardware, especially transponders. Normally a basic 10 x 10G PRBS/digital word can be used to validate continuity but a 10 Gbps per lane pattern is not transparent to a 10:4 gearbox. The mux/demux process can scramble the bit order leading to an invalid pattern. Therefore, one should have a gearbox-transparent (10 x [2 x 5 Gbps]) pattern generator that is 20 logical lanes each with a 5G PRBS (or digital word) bit-sequence muxed onto 10 physical lanes. However, the 40G (4 x 10 Gbps) does not require this.

The test should start with a short PRBS (2^{7-1}) and move to a longer pattern if everything runs well. The ONT 100G test set reports both errored zeros and errored ones as well as the conventional error count. This capability is useful for determining error bias, which can be an indication with some photonic automatic gain control (AGC) circuits. Longer patterns and digital words can also be used to stress clock recovery and direct current (DC) balance aspects of the circuitry. The ONT 100G also allows for offsetting the PRBS patterns (per lane) to remove any bit-wise correlation between lanes that could mask any potential crosstalk issues.

Lambda mapping is another unique and powerful tool that the ONT 100G provides that allows mapping of individual 5 Gbps PRBS to the 25G lambda that carries it (via the gearbox). This mapping is random at start up and can change on the Rx or Tx upon loss of clock signal; therefore, users cannot predetermine it. However, the ONT has a patented algorithm that can determine it, allowing the end user to determine if errors are correlated with a 10G lane (electrical issue) or a 25G lambda (photonic issue). See Figure 6 for a screen illustrating the lambda mapping BERT.

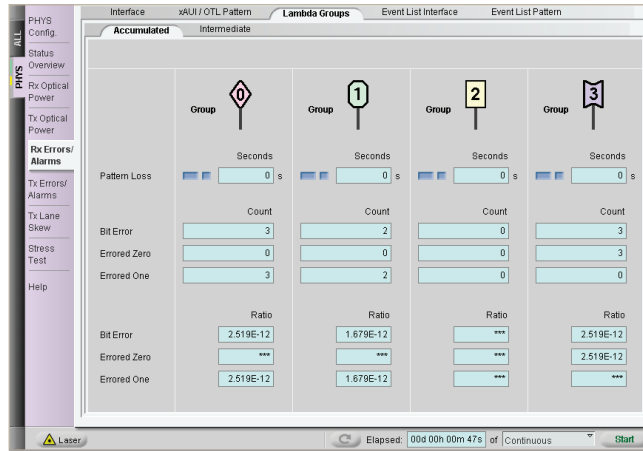


Figure 6. The Lambda mapping BERT screen

Voltage Swing and Pre-Emphasis Margin

Control over the voltage swing can allow margin testing on the electrical interface as well as the use of the ONT electrical CFP adapter to drive longer electrical cables. With this combination, the 100G Attachment Unit Interface (CAUI) (or 40G AUI [XLAUI]) electrical reference plan can be extended out (by up to 1 m), which places the CFP under test in a climatic chamber while conducting the full range of tests to allow testing over the full range of nominal operating temperature. Full and precise control over voltage swing and pre-emphasis allows use of the electrical adapter to its full advantage, as Figure 7 illustrates.



Figure 7. The CFP electrical adapter maintains electrical access to all the high-speed CAUI/XLAUI signals.

Dynamic Skew

Skew (timing variation) between lanes can become an issue with any parallel data bus. At 10G per lane, only 100 ps exists per UI, so even a small change in timing per lane may represent a significant part of the whole UI. The ONT allows for controlling two types of skew variation. The first is controlling a variation on the whole UI on a per-lane basis, which is the standard static skew approach. The first skew variation provides a useful indication (at the PCS layer) of the performance of the per lane first-in/first-out (FIFO) buffer depth. More critical is the performance of the receiver tolerance to dynamic skew variation. If a link has been established, then the 10(4) individual lanes must continue to track correctly despite skew changes across a range of ± 2 UI. This dynamic skew tolerance ensures that any propagation delay variation in individual 10G output buffers will not cause bit errors in the line receivers.

Figure 8 shows, the control screen for the dynamic skew variation test that allows individual lanes to be subject to dynamic skew variation (in steps of 25 mUI out to ± 16 UI). Compensation for the variation in the skew of the transmitted lanes is provided by the receiver FIFO/data link layer (DLL) circuitry. If the variation is too large, the receiver slip causes a bit error. The dynamic skew test is a mandatory test called out in IEEE 803.3ba.

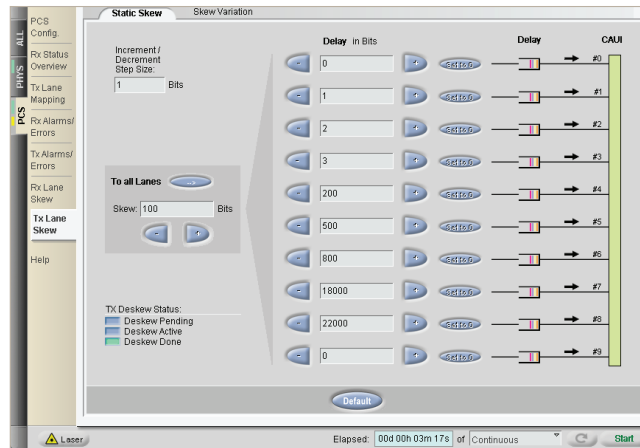


Figure 8. Dynamic Skew Control Screen – Individual lanes can be varied in 25 mUI steps

Skew Tolerance Skew Point	Maximum Skew	Maximum Skew Variation
SP1	29 ns (~150 UI)	0.2 ns (~ 2 UI)
SP2	43 ns (~222 UI)	0.4 ns (~ 4 UI)
SP3	54 ns (~278 UI)	0.6 ns (~ 6 UI)
SP4	134 ns (~691 UI)	134 ns (~691 UI)
SP5	145 ns (~748 UI)	3.6 ns (~ 37 UI)
SP6	160 ns (~824 UI)	3.8 ns (~ 39 UI)
At PCS RX	180 ns (~928 UI ~928 bits)	4 ns (~ 41 UI 41 bits)

(SP points shown in Figure 9 of the multilane model.)

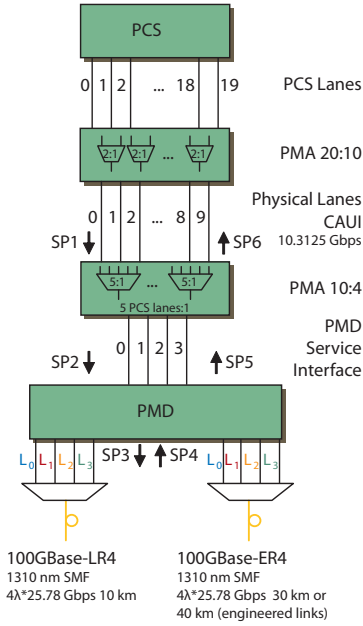


Figure 9. Multilane model

MDIO Compliance

The MDIO serial control also demands attention (as Figure 10 shows), because the in-depth features it supports require validation for performance over a range of operating conditions. Some implementations of MDIO based on slower microcontrollers within the CFP may struggle to keep up with features such as auto-increment address. It is also important that parameters such as optical power, temperature, voltage, and vendor ID are correctly identified. The ONT offers a suite of MDIO debug applications and includes several MDIO operating modes that allow control over a CFP even with MDIO issues. The static control and monitoring lines should also be checked for operation, because the programmable control lines are often used by CFP vendors for special functions specific to their CFP.

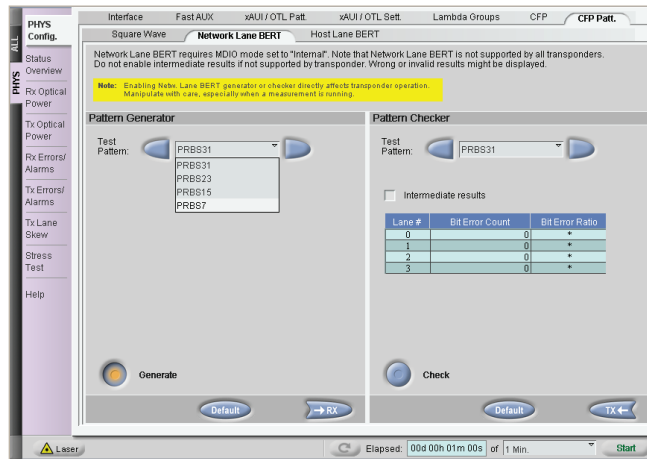


Figure 10. MDIO serial control demanding attention

Stress Testing

The ability to fully stress test the range of parameters such as dynamic skew and clock pulling range automatically is extremely valuable in screening components for production; such an automated test can be used together with climatic chambers to give complete confidence in module performance. As Figure 11 shows, the ONT is unique in that it offers a fully automatic ‘canned’ stress test for CFPs.

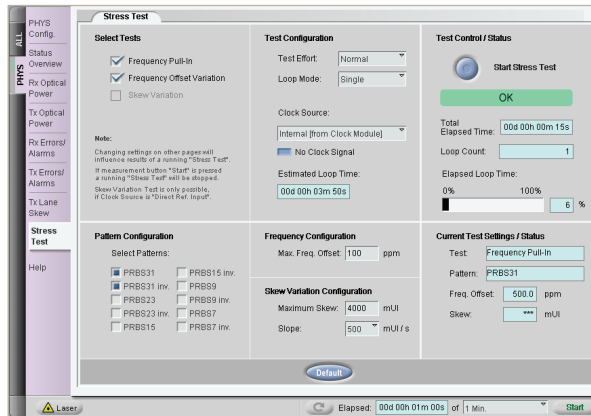


Figure 11. Automatic Stress Tests for CFPs

Summary

CFPs remain the critical path for cost-effective and reliable 100GE deployment; and as dual rate (100 GE and OTU4/111.8 Gbps) CFPs are developed, they will also require extensive testing and characterization. They are complex and involve interaction between fast photonics, parallel electronics, and firmware.

It is prudent to validate all aspects of CFP performance, not just the classic link BER. The parallel data means inter-lane timing and pattern sensitivity and crosstalk must all be thoroughly stressed before deployment. Having breadth and depth of test coverage for CFPs coupled with applications that quickly help highlight and troubleshoot issues is mandatory for quick and cost-effective product release. The JDSU ONT offers complete coverage from the physical layer through the photonics and PCS/Ethernet traffic into deep OTN analysis with many unique and valuable features, such as dynamic skew. An investment in test equipment that can cover the whole 40/100 GE and OTU3/4 needs, from component and IP selection, through optics validation and into system test and deployment makes more sense than ever.

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